AMENDMENTS TO THE CLAIMS

1. (Original) Apparatus for creating a low-bandwidth channel in a high bandwidth channel comprising:

a deserializer converting a serial high bandwidth channel from a serial datastream to an output high bandwidth parallel datastream,

memory holding an extra packet for the low-bandwidth channel,

memory holding the high bandwidth parallel datastream while the packet for the low-bandwidth channel is being sent,

a serializer converting a parallel datastream to a serial datastream, and

control logic accepting the high bandwidth parallel datastream, the control logic routing the high bandwidth parallel datastream to the serializer when the extra packet is not being transmitted and routing the output of the memory holding the extra packet to the serializer while transmitting the extra packet forming the low bandwidth channel.

2. (Original) The apparatus of Claim 1 where the control logic uses a state machine.

3. (Original) The apparatus of Claim 1 where the memory holding the high bandwidth parallel datastream is organized as a first-in-first-out memory.

4. (Currently Amended) ~~The apparatus of Claim 1~~ Apparatus for creating a low-bandwidth channel in a high bandwidth channel comprising:

a deserializer converting a serial high bandwidth channel from a serial datastream to an output high bandwidth parallel datastream,

memory holding an extra packet for the low-bandwidth channel,

memory holding the high bandwidth parallel datastream while the packet for the low-bandwidth channel is being sent,

a serializer converting a parallel datastream to a serial datastream, and

control logic accepting the high bandwidth parallel datastream, the control logic routing the high bandwidth parallel datastream to the serializer when the extra packet is not being transmitted and routing the output of the memory holding the extra packet to the serializer while transmitting the extra packet forming the low bandwidth channel, where the control logic includes:

a first multiplexer selecting between the output of the extra packet memory and the output of the first-in-first-out memory,

a second multiplexer selecting between the output of the deserializer and the output of the first multiplexer, the output of the second multiplexer feeding the serializer.

5. (Currently Amended) ~~The apparatus of Claim 3 further comprising:~~ Apparatus for creating a low-bandwidth channel in a high bandwidth channel comprising:

a deserializer converting a serial high bandwidth channel from a serial datastream to an output high bandwidth parallel datastream,

memory holding an extra packet for the low-bandwidth channel,

memory holding the high bandwidth parallel datastream while the packet for the low-bandwidth channel is being sent, where the memory holding the high bandwidth parallel datastream is organized as a first-in-first-out memory;

a serializer converting a parallel datastream to a serial datastream,

control logic accepting the high bandwidth parallel datastream, the control logic routing the high bandwidth parallel datastream to the serializer when the extra packet is not being transmitted and routing the output of the memory holding the extra packet to the serializer while transmitting the extra packet forming the low bandwidth channel;

a register controlled by the control logic, the input of the register connected to the deserializer output,

a first multiplexer controlled by the control logic, the first multiplexer selecting between the memory holding the extra packet and the register output,

the output of the first multiplexer feeding the first-in-first-out memory,

and a second multiplexer controlled by the control logic, the second multiplexer selecting between the output of the register and the output of the first-in-first-out memory,

the output of the second multiplexer feeding the serializer.

6. (Original) The apparatus of Claim 3 where the memory holding the extra packet for the low-bandwidth channel is a portion of the first-in-first-out memory.

7. (Original) The apparatus of Claim 1 where the serializer has an optical output.

8. (Original) The apparatus of Claim 1 where the serializer has an electrical output.

9. (Original) A method of creating a low-bandwidth channel in a high-bandwidth channel comprising:

converting the high-bandwidth serial channel to a high bandwidth parallel datastream,

holding an extra packet for the low-bandwidth channel in a memory,

capturing the high bandwidth parallel datastream in a memory while the packet for the low bandwidth channel is being sent, and

selecting under control of a state machine either the high bandwidth parallel datastream or the extra packet in the low bandwidth channel memory for conversion 25 from parallel to serial form.

10. (Original) The method of Claim 9 where the conversion from parallel to serial form produces an optical output.

11. (Original) The method of Claim 9 where the conversion from parallel to serial form produces an electrical output.

12. (New) The apparatus of Claim 4 where the control logic uses a state machine.

13. (New) The apparatus of Claim 4 where the memory holding the high bandwidth parallel datastream is organized as a first-in-first-out memory.

14. (New) The apparatus of Claim 13 where the memory holding the extra packet for the low-bandwidth channel is a portion of the first-in-first-out memory.

15. (New) The apparatus of Claim 4 where the serializer has an optical output.

16. (New) The apparatus of Claim 4 where the serializer has an electrical output.

17. (New) The apparatus of Claim 5 where the control logic uses a state machine.

18. (New) The apparatus of Claim 5 where the memory holding the high bandwidth parallel datastream is organized as a first-in-first-out memory.

19. (New) The apparatus of Claim 18 where the memory holding the extra packet for the low-bandwidth channel is a portion of the first-in-first-out memory.

20. (New) The apparatus of Claim 5 where the serializer has an optical output.

21. (New) The apparatus of Claim 5 where the serializer has an electrical output.